Notice of References Cited	Application/Control No. 09/847,138	Applicant(s)/Patent Under Reexamination VEILLETTE, BENOIT R.	
	Examiner Eduardo Garcia-Otero	Art Unit 2123	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-5,647,365	07-1997	Abboud, William J.	600/447
*	B	US-5,905,692	05-1999	Dolazza et al.	367/123
*	C	US-5,922,962	07-1999	Ishrak et al.	73/632
*	D	US-5,322,068	06-1994	Thiele et al.	600/447
*	E	US-5,068,833	11-1991	Lipschutz, David	367/98
*	F	US-4,821,706	04-1989	Schleicher et al.	600/437
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"HDL Chip Design" by Douglas J. Smith, Doone Publications, 1996, ISBN 0-9651934-3-8, pages 2-19.
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.